INTEGRATED GHz VOLTAGE CONTROLLED OSCILLATORS

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Abstract

The voltage controlled oscillator (VCO) is a critical sub-block in communications transceivers. The role of the VCO in a transceiver and the VCO requirements are first reviewed. The necessity of GHz VCOs and the driving factors towards the monolithic integration of the VCO are examined. VCO design techniques are outlined and design trade-offs are explored. The performance of VCOs in different implementation styles is compared to evaluate when and if VCO integration is desirable.

1 Introduction

The last decade of this century has seen an explosive growth in the communications industry. People want to be connected all the time using wireless communication devices. In addition, the demand for high bandwidth communication channels has exploded with the advent of the internet. Thanks to the high density available on integrated circuits, sophisticated digital modulation schemes can be employed to maximize the capacity of these channels. This has changed the design of wireless and wireline transceivers. We focus on the design of a critical sub-block: the voltage controlled oscillator (VCO). We review the requirements for VCOs and evaluate the advantages and disadvantages of VCO integration.

Voltage controlled oscillators appear in many analog and RF signal processing systems. In this paper we focus on silicon implementations of VCOs for communication applications. First we focus on the three parts of the title: we investigate what the role of a VCO is in a transceiver and discuss the requirements for a VCO by reviewing a typical VCO data-sheet; next, we focus on the necessity of GHz VCOs; and finally, we look into what drives the demand for integrated VCOs.

The trade-offs and techniques for VCO designs are then reviewed and relations between noise performance and power consumption are investigated. The performance of VCOs realized in different implementation styles is compared and finally we try to evaluate if or when integrated GHz VCOs are desirable.

2   Why an Integrated GHz VCO ?

2.1   Why a Controllable Oscillator ?

Most electronic signal processing systems require frequency or time reference signals. To use the full capacity of communication channels, e.g. wireless, wired and optical channels, transmitters modulate the baseband message signal into different parts of the spectrum to exploit better propagation characteristics or to frequency multiplex several messages, and the receivers downconvert them for demodulation. These operations require accurate frequency reference signals. Digital circuits and mixed mode circuits (A/D and D/A converters e.g.) pace and synchronize their operations using a clock signal as a time reference signal.

For the lower end of the spectrum one can use the stable properties of quartz crystals as a resonator to build very accurate fixed frequency or time reference signals. For higher frequencies (> few hunderd MHz) the quality of the crystal resonators degrades due to physical limitations and material properties. Many communications applications require programmable carrier frequencies and the cost and board space of a multitude of crystals would be prohibitive. Indirect frequency synthesis techniques based on a phase-locked-loop (PLL) [1] are preferred to generate programmable carriers and RF frequencies. A less accurate RF oscillator whose frequency can be controlled with a control signal is embedded in a feedback loop and its output frequency is locked to an accurate low frequency reference. These loops are typically implemented as a phase-locked-loop as shown in figure 1.

Two basic types of controlled oscillators exist: voltage controlled oscillators (VCO) with a voltage control signal and current controlled oscillators (ICO) with a current control signal. Whereas we will mainly refer to VCOs in the remainder of the text most concepts are equally applicable to ICOs.

In some instances like data communications, the data rate is very accurately standardized. Still a local clock signal is derived from the incoming data signal with a clock recovery circuit to track small variations in the senders clock rate and to align the phase of the local clock for optimal data recovery [2]. This again requires an oscillator whose frequency is controllable.
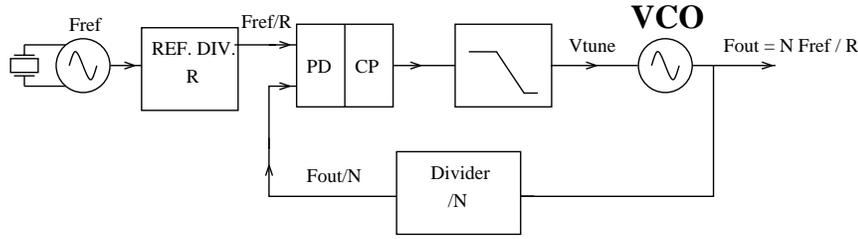
Figure 1: A phase locked loop consists of a voltage controlled oscillator (VCO), frequency divider, phase detector (PD), charge pump (CP) and lead-lag loop filter; the VCO's output frequency F_{out} is set to a multiple of the reference oscillators frequency F_{ref} depending on the divider ratios (N & R).

Another important application of VCOs is for the modulation or demodulation of frequency or angle modulated carriers. Open loop modulation and demodulation as well as closed loop schemes are very popular for portable wireless handsets [3, 4]

2.2 VCO Spec-sheet

Apart from a controllable frequency we now review the other requirements for VCOs; the specification sheet of a VCO typically has the following entries:

Center Frequency: is the output frequency f_0 of the VCO with its control voltage at its center value and is expressed in [Hz]. In this paper we use f_0 or its angular frequency equivalent $\omega_0 = 2\pi f_0$ in [rad/sec] interchangeably.

Tuning Range: is the range of output frequencies that the VCO oscillates at over the full range of the control voltage.

Tuning Sensitivity: is the change in output frequency per unit change in the control voltage, typically expressed in [Hz/V]. VCOs intended for frequency synthesis applications can have a nonlinear relationship between control voltage and oscillation frequency so that several values are quoted or min/max boundaries are given. VCOs for (de)modulation will quote the linearity of the tuning input and the bandwidth of the tuning input.

Spectral Purity: can be specified depending on the application, in the time domain in terms of jitter or in the frequency domain in terms of phase noise or carrier/noise ratio.

Load Pulling: quantifies the sensitivity of the output frequency to changes in its output load. In some applications the output load of the VCO is switched while the VCO must remain at the same frequency to avoid frequency errors
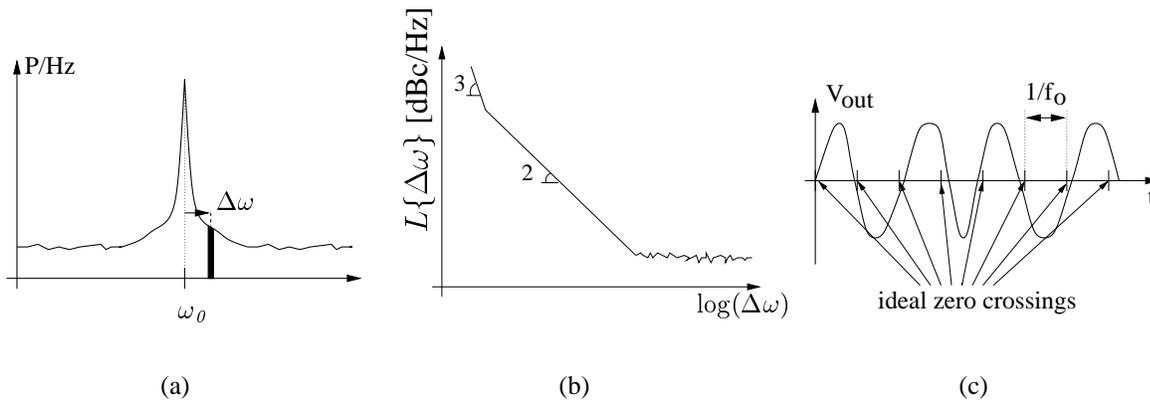
Figure 2: (a) Due to noise sources in the oscillator the output spectrum is not an ideal tone but has noise side bands and a wide-band noise floor; (b) typical plot of phase noise side band as a function of frequency offset from the carrier; (c) in the time domain the zero crossings are not equally spaced because of the effect of phase noise.

when in open loop or to avoid transients in the PLL. This spec depends strongly on the isolation provided by the output stage in the oscillator.

Supply Pulling: quantifies the sensitivity of the output frequency to changes in the power supply voltage and is expressed in [Hz/V]. The power up or down of other circuits can create significant transients in the power supply voltage and it is again desirable that the VCO frequency remains undisturbed.

Power Consumption: specifies the DC power drain by the oscillator and its output buffer circuits.

Output Power: is the power the oscillator can deliver to a specified load. The variation of the output power over the tuning range is also specified.

Harmonic suppression: specifies how much smaller the harmonics of the output signal are compared to the fundamental component and is typically expressed in [dBc].

Spectral Purity

The meaning and relevance of most of the specs is clear from their definition. The spectral purity however requires further discussion especially since it is the key performance measure of a VCO together with its power consumption. Noise sources - thermal, 1/f, supply or substrate interference - cause changes in the amplitude and frequency of oscillation so that the output spectrum of the oscillator is not a pure tone but has noise sidebands (see fig.2(a) and 2(a)); in the time domain this means that there is an amplitude variation and that the zero-crossings of the output waveform are not perfectly equally spaced in time

but they exhibit random variations around a nominal value (see fig.2(c)) which are referred to as jitter [5, 6, 7].

The power in the noise sidebands is important for wireless receiver and transmitter applications. The close-in sidebands result in spurious responses of the receiver to nearby interfering channels or blockers [3]; they also contribute to the degradation of the modulation accuracy of the transmitter. The far-out sidebands must be low enough to reduce the spurious emissions by the transmitter to relax its output filter requirements.

The jitter in the zero-crossings of the output waveform of a phase-locked-loop is partly due to the noise or spurious sidebands of the VCO but a large contribution comes from the noise of the other components in the loop. Jitter is a limiting factor in data communications applications since it closes the eye in the eye diagram and so it makes data detection more error prone. In digital circuitry timing jitter reduces the timing margin. For mixed mode applications jitter must be small enough not to affect the accuracy of A/D or D/A conversion e.g.

There are several measures to quantify timing jitter and phase noise which are all mathematically related to each other [5, 7, 6]. In this paper we will use the characterization of the phase noise from the RF spectrum; the RF output power spectrum of an oscillator at ω_0 is symmetrical and the noise in one sideband in a 1Hz bandwidth is used to define $L_{\text{total}}\{\Delta\omega\}$:

$$L_{\text{total}}\{\Delta\omega\} = \frac{\text{noise power in 1Hz BW at } \omega_0 + \Delta\omega}{\text{total carrier power}} \quad (1)$$

In this form L_{total} depends on the effect of phase and amplitude variations. In many circuits the effect of amplitude variations can be eliminated by passing the signal through an explicit or implicit limiting stage but the effect of phase variations cannot be reduced. For most applications only the phase portion L_{phase} of L_{total} is important and is denoted as $L\{\Delta\omega\}$. Figure 2(b) shows the typical phase noise sidebands in an oscillator as a function of the frequency offset from the carrier. White noise sources give rise to a $\Delta\omega^{-2}$ dependence of the phase noise power on frequency offset whereas the $\Delta\omega^{-3}$ dependence is due to the effect of 1/f noise sources in the oscillator [8, 9, 10, 11].

2.3   Why Gigahertz Operation ?

Several evolutions push for the realization of VCOs with center frequencies in the GHz to several GHz range. In the wireless arena, the better propagation characteristics and the larger available bandwidth in the 1 to 2 GHz range have

allowed the standardization and exploitation of digital cellular phone systems worldwide. For the fabrication of the wireless phone terminals a large demand for high performance GHz VCOs has emerged. At higher frequencies around 2.5 GHz and 5 GHz new wireless data applications have spurred a lot of interest and large markets are emerging: e.g. short range automation applications in the home, cable replacement wireless links etc.

With the constant shrinking of feature sizes in IC technologies and the increase in clock speeds we are very close to the widespread use of digital systems with clock speeds in the 1 GHz range. The distribution and synchronization of those GHz clocks is very challenging and will rely on on-chip PLL clock multipliers. Already today at clock frequencies of several hunderd MHz these techniques are being used [2]. These applications will also drive the requirement for GHz VCOs.

The same trend exists in data communications were widespread deployment of Gbit/sec data channels is fueled by the Internet growth and the convergence of data and voice communications. These systems rely on clock recovery architectures and also increase the demand for GHz VCOs. It is beyond doubt that GHz VCOs are required in large volumes.

2.4   Why Integrate the Oscillator ?

High volume markets are governed by the *P words*: price - package - performance - power. IC integration reduces production cost since it allows for mass volume production. Integration of the RF components reduces the number of RF pins and thus allows for cheaper packaging solutions. However, integration increases the complexity of the part and thus testing cost/complexity can become a limiting factor or the number of I/O pins can become large which are counterproductive for packaging cost reduction. For low cost and large volume production post-fabrication trimming is to be avoided. By (partly) integrating the VCO on the IC complex automatic calibration techniques become feasible since their is an abundance of cheap active devices along with sophisticated computing power.

Performance is a key factor. In applications governed by standards, meeting the performance specifications is a 'conditio sine qua non'; without standard compliance price, package or power consumption are irrelevant. The benefit of integration for performance is less obvious when the RF functions are combined with the other digital signal processing blocks. This is because the choice of IC technology is driven by the requirements of the majority of the circuits which are digital making the cost of special technology options which enable

better analog/RF performance unjustifiable. Consequently integration typically results in a somewhat lower performance of the VCO. In the next section we evaluate the crucial circuit components in a VCO design and how they are affected by integration. Also, we make a comparison of the performance of VCOs implemented at different levels of integration and try to point out if integration makes sense. Power consumption is one of the key performances measures that is discussed.

3 Integrated GHz VCO Design

In this section the design of integrated GHz VCOs is discussed. We look at the different ways to realize a VCO and the design trade-offs between phase noise and power consumption. The design of tuned oscillators is reviewed in detail.

3.1 Classes of VCOs

Oscillators are autonomous circuits that produce a stable periodically time varying waveform. They have at least two states and they cycle through those states at a constant pace. There are three different topologies for controlled oscillators on silicon ICs: ring oscillators, relaxation oscillators and tuned oscillators [3]. Ring oscillators consist of an odd number of single-ended inverters or an even/odd number of differential inverters with the appropriate connections. Relaxation oscillators alternately charge and discharge a capacitor with a constant current between two threshold levels. Tuned oscillators contain a passive resonator - LC tank, transmission line resonator, crystal, SAW - that serves as the frequency setting element.

   The first two realizations are very easy to integrate on a monolithic IC and are very compact. Their frequency is controlled by a current or voltage and linear tuning characteristics can be obtained. Moreover, frequency tuning can be done over several orders of magnitude [12]. Tuned oscillators are harder to integrate primarily because of the lack of high quality passive inductors in standard IC technologies and because of their large size. However, tuned oscillators have a much higher frequency stability and spectral purity since it is set by the passive resonator. Relaxation and ring oscillators are typically very sensitive to noise in the switching thresholds and charging currents.

3.2   VCO design trade-offs

In this section we investigate the relation between spectral purity and power consumption of a VCO and how a large tuning range affects the design. The analysis and prediction of phase noise or timing jitter in oscillators is a very difficult task since the oscillator is an autonomous non-linear circuit and the non-linearity is essential for its operation and noise performance evaluation. Recently several techniques have been developed for the accurate simulation of phase noise in oscillators [8, 9, 10] but they are mathematically too involved to intuitively understand the trade-off between the various performance parameters.

Leeson's model [11] has long been the primary analysis and modeling tool for phase noise of oscillators. Recently, [13, 14] have presented other linear noise analyses of oscillators. Although a linear noise analysis of an oscillator has some fundamental problems and inconsistencies - like infinite noise power at the center frequency f_0 - it is analytically treatable and has given a good insight in the trade-offs between parameters.

Using approximated harmonic balance equations a more rigorous analytical derivation of the phase noise of oscillators can be performed [15]; this analysis takes into account the switching behavior of the oscillator. The results allow the evaluation of the contribution of the different noise sources and noise folding effects. Also in [16] frequency domain techniques are presented to study the effects of noise folding in oscillators.

3.2.1   Linear Noise Analysis for Parallel LC Oscillator

It will be beneficial to briefly derive the linear noise analysis of a parallel LC oscillator. First we compute the equivalent parallel resistance of the tank; then, we determine the tank impedance for small offsets from the self resonant frequency. From these results we can determine the necessary negative conductance and the carrier to noise ratio.

Figure 3(a) shows a parallel resonant LC tank with inductor, capacitor and parallel losses. We now compute the admittance of this LC configuration:

$$Y(\omega) = \frac{1}{R_p} + \frac{1}{j\omega L(1 + \frac{1}{Q_L^2})} + \frac{j\omega C}{1 + \frac{1}{Q_C^2}} + \frac{1}{Q_L \omega L(1 + \frac{1}{Q_L^2})} + \frac{\omega C}{Q_C(1 + \frac{1}{Q_C^2})} \tag{2}$$

with $Q_L = (\omega L)/R_{sl}$ and $Q_C = 1/(\omega C R_{sc})$ the inductor and capacitor quality factors respectively. Equation (2) represents an equivalent admittance with
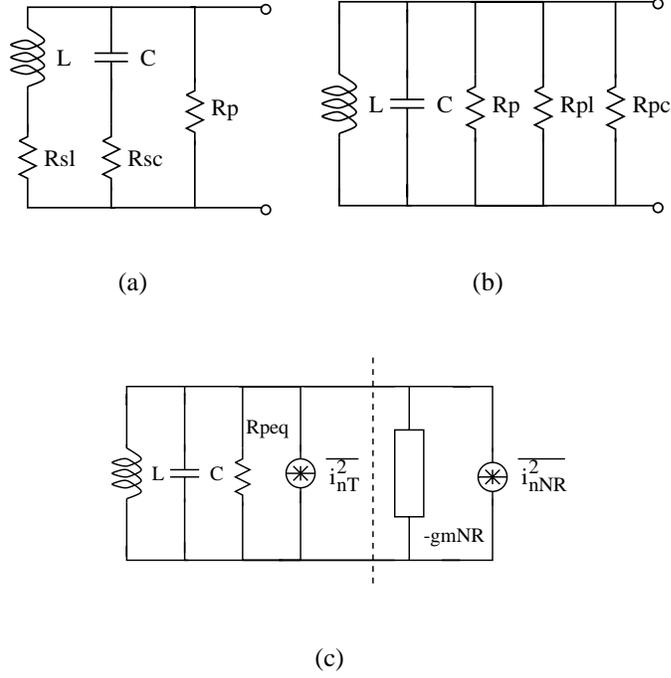
Figure 3: (a) LC tank including series losses for all components and a parallel loss; (b) equivalent LC tank with all losses represented by parallel losses; (c) parallel LC oscillator with ideal negative conductance.

3 real terms and two imaginary terms; for sufficiently large Q_L and Q_C, the tank can be represented by the equivalent circuit of figure 3(b) with $R_{pl} \approx Q_L \omega L$ and $R_{pc} \approx \frac{Q_C}{\omega C}$. It is useful to define the characteristic impedance Z_0 and the quality factor of complete tank circuit Q_T as follows:

$$Z_0 = \left(\frac{1}{\omega C} \right) = \omega L = \sqrt{\frac{L}{C}} \tag{3}$$

$$R_{peq} = R_p // R_{pc} // R_{pl} \tag{4}$$

$$Q_T = \frac{R_{peq}}{Z_0} \tag{5}$$

$$\left(\frac{1}{Q_T} \right) = \frac{Z_0}{R_p} + \left(\frac{1}{Q_L} \right) + \left(\frac{1}{Q_C} \right) \tag{6}$$

Interesting to note is that the total tank quality Q_T is determined by the lowest quality factor component.

To build an oscillator that operates the tank at its parallel resonance ($\omega_0 = 1/\sqrt{LC}$), a negative conductance is added in parallel to compensate the losses and to sustain the oscillation (see figure 3(c)). The necessary minimal negative

conductance g_{mc} is given by:

$$g_{mc} = \text{Re}\left\{Y(\omega_0)\right\} = \frac{1}{R_{peq}} = \frac{1}{Q_T Z_0} \tag{7}$$

To guarantee start-up under all conditions the negative conductance is over-designed by a factor $\alpha = 1.5 - 3$ so that $g_{mNR} = -\alpha g_{mc}$.

To evaluate the noise to carrier ratio of the oscillator we compute the tank impedance at an offset frequency $\Delta\omega$ from the oscillation frequency ω_0 from (2):

$$Y(\omega_0 + \Delta\omega) \approx 2j\left(\frac{\Delta\omega}{\omega_0}\right)\frac{1}{Z_0} + \frac{1}{R_{peq}} \tag{8}$$

In an oscillator the effect of real part in the tank admittance - the second term in equation (8) - is cancelled with the negative conductance so that only the first term remains.

We can now calculate the noise to carrier ratio; we assume a given oscillation signal V_{RMS}; the tank losses generate a noise current $\overline{i_{nT}^2} = 4kTg_{mc}$ that is transformed to a noise voltage by the tank impedance; similarly there is a contribution from the noise current of the negative conductance $\overline{i_{nNR}^2} = 4kT\Gamma\alpha g_{mc}$, where Γ is the noise excess factor of the negative conductance implementation (see figure 3(c)). At an offset $\Delta\omega$ from resonance we obtain the following $L_{\text{total}}\{\Delta\omega\}$:

$$L_{\text{total}}\{\Delta\omega\} = \frac{\overline{v_n^2}}{V_{RMS}^2} = \frac{\overline{i_{nT}^2} + \overline{i_{nNR}^2}}{|Y(\omega_0 + \Delta\omega)|^2}\frac{1}{V_{RMS}^2} \tag{9}$$

$$L_{\text{total}}\{\Delta\omega\} = kT\left(\frac{Z_0}{Q_T}\right)\left(\frac{\omega_0}{\Delta\omega}\right)^2\frac{1 + \alpha\Gamma}{V_{RMS}^2} \tag{10}$$

The classical distribution of $L_{\text{total}}\{\Delta\omega\}$ into phase and amplitude fractions assumes an equal division of the noise so that $L_{\text{phase}}\{\Delta\omega\} = L\{\Delta\omega\} = L_{\text{total}}\{\Delta\omega\}/2$ [6].

3.2.2 Design trade-offs

Figure 4(a) depicts an implementation of the parallel resonant oscillator of figure 3(c) using an nMOS differential pair negative conductance.

We can now derive the oscillation signal V_{RMS} (see also [17, 16, 18]). In figure 4(b) the voltage across the tank ($V_p - V_m$) and the currents in the negative conductance are depicted for transistors with a zero threshold voltage. In

Figure 4: (a) nMOS differential pair implementation of negative conductance; (b) voltage waveforms and current waveforms for zero threshold voltage transistors; (c) equivalent representation of (a) using current sources to model the effect of the switching transistors.

figure 4(c) the effect of the negative conductance circuit is modeled with equivalent common mode and differential mode current sources. The differential output current (I_{diff}) of the negative conductance is a square wave with amplitude $I_B/2$; the tank filters the higher order harmonics of this current signal and only its Fourier component at ω_0 $I_{\omega 0} = 2I_B/\pi$ is converted into a differential voltage by the equivalent impedance at resonance $R_{peq} = Q_T Z_0$ so that the RMS value of the differential voltage across the tank is given by:

$$V_{RMS} = \frac{1}{2\sqrt{2}} R_{peq} I_{\omega 0} = \frac{2}{\sqrt{2}\pi} I_B Q_T Z_0 \tag{11}$$

With real transistors and a real current source similar behavior occurs. Because the small signal negative conductance g_{mNR} is made ($\alpha \geq 1$) times larger than the minimal required g_{mc} to ensure start-up, the oscillator waveforms grow until the negative resistor circuit goes into a switching operation and the amplitude has a similar dependence on I_B, Q_T and Z_0 as in (11). However, the single ended peak value of V_p and V_m must be smaller than V_{DD} to keep the current source working as a current source; for increasing values of the bias current I_B the oscillator will go from a current limited operation – assumed above in (11) – to a voltage limited operation (see e.g. [18]).

The negative conductance g_{mNR} is equal to half the transconductance g_m

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of transistors M_1 and M_2 in figure 4(a), which can be expressed as: $g_m = (g_m/I)I_B/2$ with $(g_m/I) = 2/(V_{GS} - V_T)$ [19]. We now rewrite α as:

$$\alpha = \frac{g_{mNR}}{g_{mc}} = \frac{(g_m/I)I_B Q_T Z_0}{4} \tag{12}$$

so that for a fixed start-up gain α we can compute the required bias current as:

$$I_B = \frac{4\alpha}{Q_T Z_0 (g_m/I)} \tag{13}$$

The voltage swing then becomes:

$$V_{RMS} = \frac{8\alpha}{\sqrt{2}\pi(g_m/I)} \tag{14}$$

After substitution of (14) into (10) we obtain the following equivalent expressions:

$$L_{\text{total}}\{\Delta\omega\} = kT\frac{\pi^2}{32}\left(\frac{\omega_0}{\Delta\omega}\right)^2 \frac{1 + \alpha\Gamma}{\alpha^2}\frac{(g_m/I)^2 Z_0}{Q_T} \tag{15}$$

$$L_{\text{total}}\{\Delta\omega\} = kT\frac{\pi^2}{8}\left(\frac{\omega_0}{\Delta\omega}\right)^2\left(\frac{1 + \alpha\Gamma}{\alpha}\right)\frac{(g_m/I)}{Q_T^2 I_B} \tag{16}$$

Equations (15) and (16) show that the use of a large start-up gain α improves the noise to carrier ratio since increasing the start-up gain increases the noise power contribution of the negative conductance but at the same time increases the carrier power quadratically. For increasing α the $\alpha\Gamma$ in the numerator will exceed 1 and the noise contribution of the negative conductance dominates. Equation (16) can then be rewritten as:

$$L_{\text{total}}\{\Delta\omega\} \propto kT\left(\frac{\omega_0}{\Delta\omega}\right)^2\frac{(g_m/I)\Gamma}{I_B Q_T^2} \tag{17}$$

In order to arrive at equation (17) we have mixed linear analysis and large signal concepts. It is however noteworthy that more extended non-linear analyses result in a similar relation for $L_{\text{total}}\{\Delta\omega\}$ [15, 16] and the time variant noise effects and noise folding can be taken into account with a proper value for Γ in (17) [15, 16].

Equation (17) provides an important insight in the trade-off between the power consumption and phase noise of an LC oscillator: the power consumption

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Specifications	
Center Frequency:	ω_o
Phase Noise:	$L\{\Delta\omega\}$
Technology Constraints	
Resonator quality	Q_T
Design Variables	
Inductance:	L
Capacitance:	C
Tank Characteristic Impedance:	Z_0
Bias Current:	I_B
Transistor :	(g_m/I)
Design Relations	
$\omega_0 = 1/\sqrt{LC}$ $Z_0 = \sqrt{L/C}$ $\alpha = \frac{g_{mNR}}{g_{mc}} = (g_m/I)I_B Q_T Z_0/4 \geq 1 \ (12)$ $L\{\Delta\omega\} \propto kT\left(\frac{\omega_0}{\Delta\omega}\right)^2 \frac{(g_m/I)\Gamma}{I_B Q_T^2} \ (17)$	

Table 1:

is $P = I_B V_{DD}$ so the phase-noise power product ($L\{\Delta\omega\}P$) of the oscillator becomes[1]:

$$L\{\Delta\omega\}P \propto \left(\frac{\omega_0}{\Delta\omega}\right)^2 \frac{(g_m/I)\Gamma V_{DD}}{Q_T^2} \qquad (18)$$

It is desirable to minimize both sides of relation (18). Equation (18) also illustrates the importance of the quality factor of the tank circuit Q_T: a high tank quality factor results in low noise and power efficient oscillators. The quality factor is however dependent on the technology available for the fabrication of the tank and is mostly beyond the control of the circuit designer.

3.2.3 LC Oscillator Design Procedure

In table 1 the specifications, constraints, design variables and design relations are summarized for the oscillator in figure 4(a). The designer's task is to choose the appropriate values for L, C, I_B and transistor sizes (or (g_m/I)) so that the center frequency (ω_0), start-up and phase noise requirements $L\{\Delta\omega\}$ are met, with the lowest possible power consumption P.

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[1]as discussed in the previous section the phase noise $L\{\Delta\omega\}$ is a fraction of the total noise $L_{total}\{\Delta\omega\}$.

The center frequency only fixes the product of L and C but their ratio and thus the characteristic impedance Z_0 of the tank is to be chosen. A large Z_0 – large L but small C – for a given choice of bias current I_B yields a large value for V_{RMS} (11) and α (12) which is desirable. For a given start-up gain α the choice of Z_0 does *not* influence the phase noise performance $L\{\Delta\omega\}$ – see equation (16) or equation (17) for large startup gains. $L\{\Delta\omega\}$ is in first order mainly dependent on the choice of I_B (17) and on the available tank quality Q_T. To lower the phase noise the designer has to increase the bias current I_B. This can result in too large voltage swings V_{RMS} (11) over the active devices so that Z_0 must be reduced. Smaller inductors have higher self resonant frequencies and typically somewhat higher quality factors which suggests the choice of low Z_0, however at the expense of smaller voltage swings V_{RMS} and start-up gains α. The final choice of parameters is typically decided with the help of a phase noise simulator.

3.2.4   Tuneable LC Oscillator

For most applications the required tuning range for GHz VCOs is only a few percent since the application bandwidth is much smaller than the center frequency. If tuning is also used to combat the process variations typically much large tuneability is required; a fully integrated VCO e.g. will typically exhibit +/-10% center frequency variations due to on chip capacitance variations. In order to change the center frequency f_0 to build a VCO we have to change the L or the C of the tank electronically. Continuous tuneable inductors are not readily available but varactors – voltage dependent capacitors – can be built using pn junctions or MOS capacitors [20, 21]. To tune between f_{max} and f_{min} at least a fraction ΔC of the total tank capacitance C must be variable:

$$\Delta C \geq 2C\frac{f_{max} - f_{min}}{0.5(f_{max} + f_{min})} \tag{19}$$

In figure 5 the implementation of a parallel resonant LC CMOS VCO with pn varactors or MOS varactors is illustrated.

Tuneability entails three main design issues. Varactors always have a percentage of fixed capacitance associated with the variable capacitance so that the fixed tank capacitance increases. To keep the oscillation frequency high Z_0 has to be lowered which reduces the start-up gain α and the voltage swing. Secondly, varactors have a lower quality factor than fixed capacitors so that the tank quality Q_T reduces if a large tuneability is required. Thirdly, pn junction varactors have to remain reverse biased under all conditions to avoid conduc-
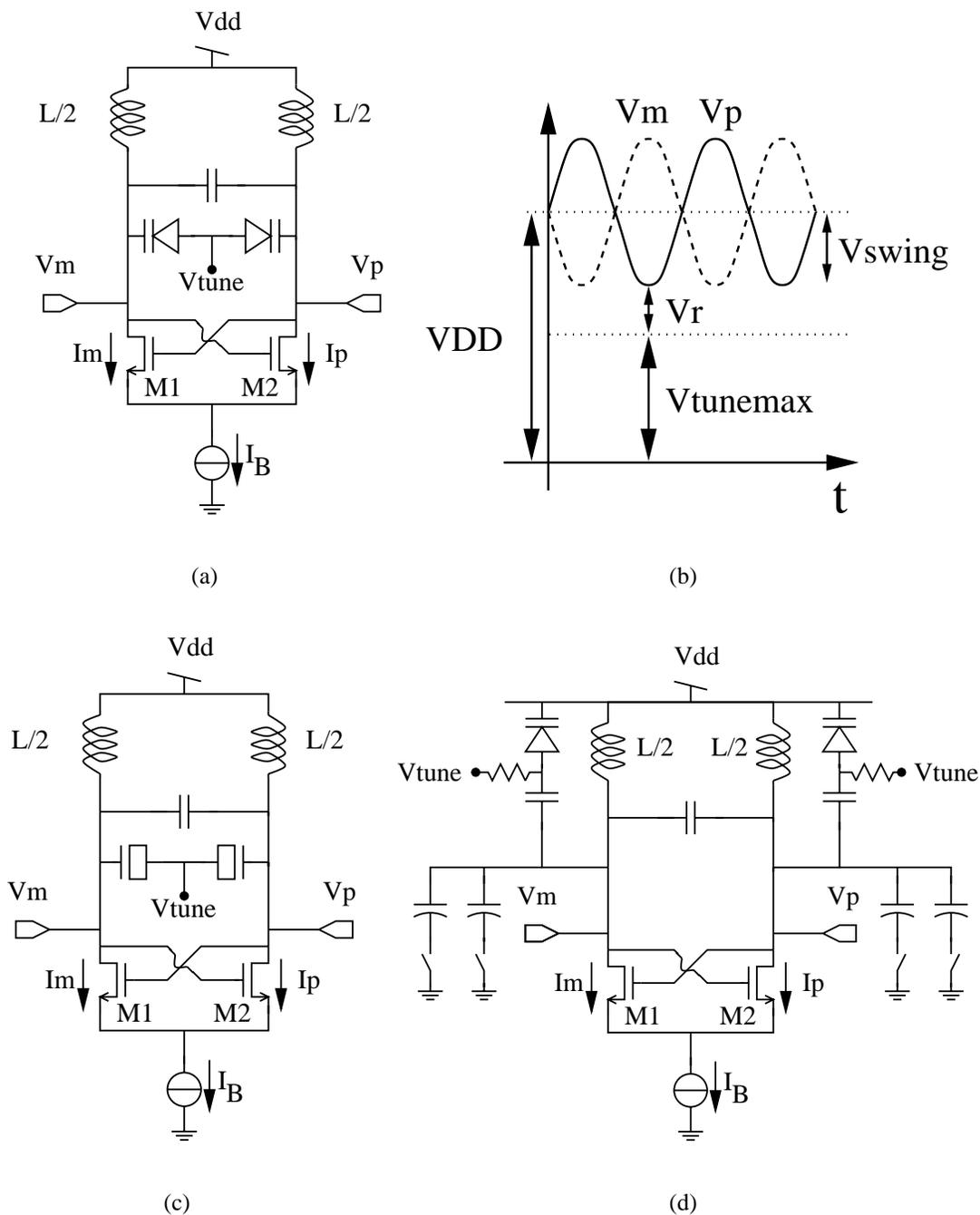
Figure 5: Modification of fixed frequency oscillator in figure 4(a) to a voltage controlled oscillator using (a) pn junction varactors, (c) MOS varactors, or (d) capacitively tapped varactors and discrete tuning capacitors; (b) shows the relation between the maximal tune voltage, diode reverse voltage, voltage swing across the tank and supply voltages.

tion losses and thus further Q_T degradation. As illustrated in figure 5(b), the maximal allowable voltage swing across the varactors for a given tuning voltage range $V_{tunemax}$ is limited by the available supply voltage V_{DD} and the minimal reverse bias across the diode V_R. MOS varactors do not have conduction losses but the voltage swing has be small enough to prevent gate breakdown; also, at larger swings across the MOS varactor the capacitance/voltage relation becomes strongly non-linear and more harmonics are generated.

The last two problems can be alleviated by capacitively tapping the varactors with fixed high Q capacitors (see figure 5(d)). Capacitive tapping results in an impedance transformation [4, 3] and the effective Q of the structure scales up with the tapping ratio but the variability of the varactor ΔC scales down with the tapping ratio[2]. If a fixed capacitor with low parasitic bottom plate and high Q is available, one can thus improve the quality of the varactor at the price of area. At the same time there is no DC connection between the tank and varactor anymore, and the voltage swings across the varactors are scaled down with the tapping ratio so the swing limitations can be remedied.

As process technologies shrink the speed f_0 of the oscillators goes up but the supply voltages scale down. The tuning gain K_V necessary to compensate process variations is ($K_V \propto 20\% \cdot f_0/V_{DD}$) since the tuning voltage must be within the supply voltage for an integrated oscillator. As the oscillator's frequency goes up and the supply voltages go down the tuning gain K_V increases. The noise voltage present at the tuning port of the oscillator results in a frequency modulation of the carrier and thus in phase noise. If we assume a resistor R at the tune port its voltage noise results in phase noise level given by:

$$L\{\Delta\omega\} = 2kTR\left(\frac{K_V}{\Delta\omega}\right)^2 \tag{20}$$

where K_V is in [rad/V]. For increasing K_V the allowable impedance level at the tuning port reduces. In the PLL design this implies a lower impedance level for the loop filter and thus larger capacitors which is counterproductive for chip integration since it increases the area of the PLL. However, the correction for the process variations does not have to be continuous but can be done with discrete tuning [22] (see figure 5(d)) and still be automated so no trimming is required [23]. This approach has the benefit that the tuning sensitivity of the tune port of the VCO is reduced for a fixed tuning voltage range so that less noise from the other PLL components appears at the output [6].

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[2]For the series connection of a variable capacitor C_V with a capacitance variation ΔC_V and a quality Q_V, and a high Q capacitor C_{tap}, one can easily obtain that the quality of the series connection is $Q_V(C_{tap} + C_V)/C_{tap}$ and the capacitance variation $\Delta C = \Delta C_V C_{tap}/(C_{tap} + C_V)$.

In summary we note that the introduction of tuneability complicates the oscillator design and consequently has negative implications on the achievable phase noise - power trade-off.

3.2.5 Transistor Sizing

For a given choice of bias current I_B an MOS designer still has to decide on the (g_m/I) of the devices. The (g_m/I) is increased by reducing the $(V_{GS} - V_T)$ at the price of a lower transit frequency f_T ($f_T = g_m/C_{gs}$) of the device [19]. Lower device f_T implies larger capacitive loading by the negative resistance of the tank. These capacitors become part of the tank circuit and the Q of the total tank circuit is then typically denoted as the 'loaded Q' of the oscillator. For high Q tanks is important to keep the transistor parasitics small to avoid degradation of the loaded Q due to the lower quality parasitics. For low Q fully integrated tanks the quality factor of the transistor parasitics can be high enough so that the parasitics can be used as the main part of the tank capacitance and high frequency operation can be achieved [24].

Equation (17) suggests lowering (g_m/I) values to improve the noise performance of the oscillator since a low (g_m/I) results in less noise current for the same bias current I_B. But low (g_m/I) also results in lower start-up gains α (12) and linearizes the negative conductance which results in a reduction of the oscillation amplitude for the same bias current I_B. This causes an increase in the noise to carrier ratio of the oscillator. These effects can be balanced by investigating the best choice for (g_m/I) with a phase noise simulator.

Bipolar devices have a fixed (g_m/I) [19]. The device size is primarily determined by the maximal allowable current density or the base spreading resistance. To reduce the base resistance larger emitter areas and finger layouts are used but this results in the operation of the device below its 'peak f_T'. The parasitic capacitive loading of the tank can become significant and the loaded Q_T can reduce if the tank characteristic impedance was chosen too high.

3.2.6 Other configurations

There a several more oscillator configurations that are well suited for integrated circuit implementations see e.g. [3, 4]. Colpitts configurations are very well established and are very popular for single-ended and bipolar designs. The design trade-offs for those configurations are similar or identical to the ones outlined above.

4 Comparison of VCO implementation styles

There are four major implementation styles for tuned VCOs. Traditionally they are implemented with hybrid modules which are easy to use but are bulky and expensive. A realization with a discrete RF device on the transceiver PCB is more cost effective but requires large board area. A third alternative is to integrate the active parts of the VCO on the transceiver chip and use external resonators. Fully integrated realizations have recently received a lot of (research) attention.

In table 2 the performance of different oscillators implemented with different technologies is listed. Their center frequencies f_0 are different and the phase noise $L\{\Delta f\}$ is specified at different offset frequencies Δf. Equation (17) or more generalized considerations [3] suggest the definition of a figure of merit FM for an oscillator that is independent of its specific oscillation frequency:

$$FM = 10 \log \left(\left(\frac{f_0}{\Delta f} \right)^2 \frac{1}{L\{\Delta f\}P} \right) \tag{21}$$

In table 2 FM is given based on P in [mW]. The power consumption P is for the oscillator core only and does not include the output buffer; when only total power consumption numbers were available the core is assumed to account for 1/3 of the total power consumption. For integrated oscillators the number of available metal layers in the process or the availability of a thick metal layer (T) is listed along with the type of substrate material: HR indicates a high resistivity substrate and LR a low resistivity substrate. The types of inductors are inte(grated), discr(ete), bondw(ire) or MCM (on multi-chip-module). Where available the inductor and varactor quality factors QL and QV are given.

In figure 6 the figure of merit is plotted against the oscillation frequency for the different group of implementation styles. A number of interesting observations can be made:

- The *ring and relaxation oscillators* consistently have a very low FM ("Ring-/Relax" in figure 6). This is due to their high noise sensitivity because of the lack of a frequency selective network. Moreover in these non-tuned oscillators, large currents flow through the active devices at the zero-crossings of the oscillation waveform and thus large noise injection occurs around the zero-crossings. Non-linear phase noise simulations [9, 10] show that the oscillator's phase is most sensitive to noise injection close to the zero-crossings.

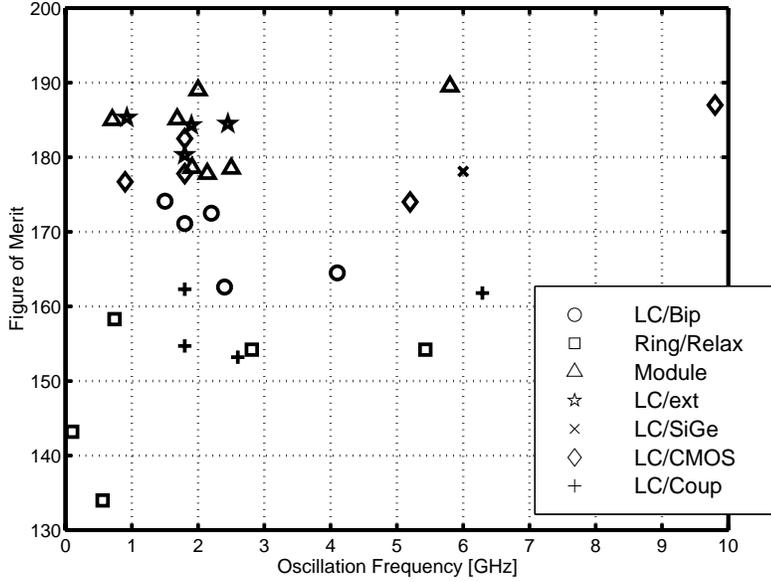 The ring and relaxation oscillators are fully integrated oscillators and oc-

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Figure 6: Comparison of the 'Figure of Merit' for several oscillators using different implementation styles

cupy much smaller chip area than integrated tuned oscillators. Ring oscillators also easily provide multi-phase output signals. Because of their compactness ring oscillators are preferred in PLLs for digital clock generation and for clock and data recovery circuits for some data communication applications. Moreover large PLL loop bandwidths can be used in these fixed frequency applications so that the effect of the VCO phase noise on the output jitter is largely reduced [7].

Interestingly the jitter requirements in data communications and digital applications are specified in unit-interval units which are relative units [5]. The jitter requirements in unit-intervals are typically kept almost unchanged when the bit rates are scaled up to conserve timing margins. The relation between the RMS jitter Δt_{RMS} and phasenoise of the PLL $L\{\Delta\omega\}$ is given by [7]:

$$\left(\frac{\Delta t_{RMS}}{T}\right)^2 = \int_{\omega_L}^{\omega_H} 2 \cdot L\{\Delta\omega\} \cdot \mathrm{d}\Delta\omega \qquad (22)$$

where T is the period, and $\omega_H - \omega_L$ is the jitter bandwidth. Equation (22) shows that the phase noise requirements $L\{\Delta f\}$ are related to the jitter requirements in unit-intervals $(\Delta t_{RMS}/T)$ so that for constant jitter requirments in unit-intervals the phase noise requirement $L\{\Delta f\}$ remains the same even when the center frequency f_0 has scaled up since the jitter bandwidths do typically not scale as much as the center frequencies. Higher
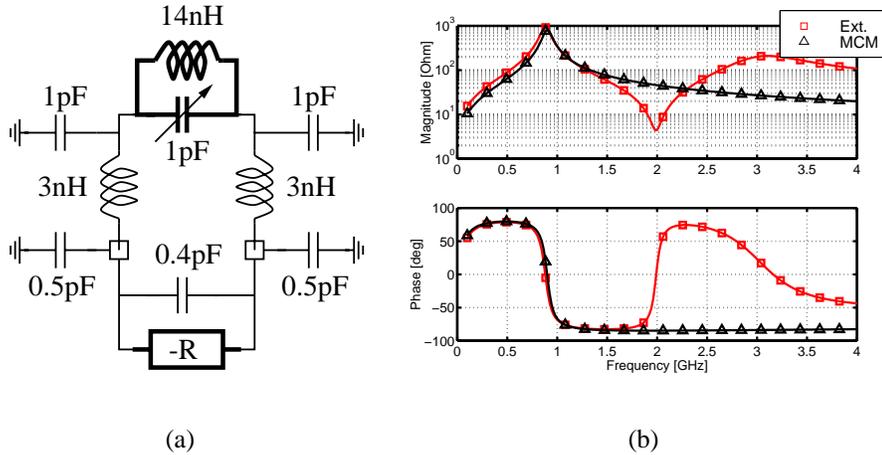
19

Figure 7: Typical example of possible spurious oscillations for a 900MHz oscillator with external tank. (a) The connection to the external tank (bold: 14nH and 1pF) from the negative resistor (-R) with its parasitic parallel capacitance (0.4pF) goes through on-chip pad capacitance (0.5pF), bondwires (3nH), and board capacitance (1pF). (b) (square) Besides the wanted parallel resonance at 900MHz, a spurious series resonance at 2 GHz and a spurious parallel resonance at 3.2 GHz exist and can be exited; (b) (triangle) if an MCM or on-chip inductor is used the spurious resonances are eliminated.

bit rate applications thus require PLLs using oscillators with higher FM, or more power needs to be dissipated in the oscillator as indicated by (21). Consequently, higher Q oscillators are (or soon will be) required for the Gbit/sec data communications clocks and digital clocks.

- The *hybrid modules* have farmost the best performance ("Module" in figure 6). They are built with the mix of the best technologies for the tank circuit, varactor and active device and typically use trimming to adjust the center frequency. Whereas they are easy to use, they are large and occupy a lot of board space and are expensive.

- The VCOs built with integrated active components and *external inductors* (discrete, MCM, bondwire) ("LC/ext" in figure 6) also have very good specifications and perform close to the hybrid modules. External inductors have significantly better quality factors than integrated inductors which is the primary reason for the higher FM.

In order to access the external resonator pins have to be reserved which complicates packaging. Also, coupling between pins or bonding wires as well as coupling on the external PCB can introduce extra interference into the oscillator or can cause unwanted leakage of the large oscillator signal to sensitive nodes in the system.

For oscillation frequencies in GHz range the tank inductance is at most a

few nanohenries to tens of nanohenries. The package lead and bondwire parasitic series inductance are however of the same order of magnitude. In some cases, the high inductance with high Q of bondwires can also be used to the designers advantage by using a bondwire as the tank inductor [13]. With external resonators, the parasitic series inductances and parasitic parallel pin and pad capacitances introduce several spurious resonances in the tank circuit which can result in unwanted modes of oscillation [25] as is illustrated in figure 4. This problem is largely reduced when more advanced packaging techniques are employed such as flip-chip mounting of the silicon die on an MCM - multi-chip-module - substrate. The lead inductance and pad capacitance is greatly reduced and the bondwire inductance is eliminated. Additionally, high quality inductors realized on the MCM substrate can be used for the tank resonator [25, 26]. The use of more advanced packaging increases the packaging cost but enables higher performant RF circuitry and allows the combination of dies in different IC technologies for different parts of the system for optimal performance. The high isolation between the separate dies is an additional benefit.

- The performance of *fully integrated VCOs* strongly depends on the available inductor quality ("LC/CMOS" and "LC/Bipolar" in figure 6). This is not surprising since equation (18) indicates a quadratic dependence on the tank quality factor. Integrated tuned oscillators use planar spirals in the available metal layers to build an inductor[4] (see figure 8). Most standard digital CMOS processes use epi-wafers which consists of low resistive p++ material with a thin lightly doped p-epi layer for the circuitry. The magnetic field of the spirals extends into the substrate and large eddy currents flow which result in a severe degradation of the inductor quality to only 3–5. This low inductor Q limits the overall tank quality to very low values [24]. Some digital CMOS processes and most BiCMOS processes have a high resistivity wafer material so that better inductor quality is achieved. The quality factor is then mainly degraded by the resistive losses in the metalization so that some RF IC technologies have the option of a special thick metalization level to build high Q inductors (QL 10–20). In table 2 the performance of fully integrated MOS LC oscillators is indeed typically better for the high resistivity processes. It is also very promising that the MOS LC oscillators perform well compared to oscillators with external tanks.

Fully integrated tuned VCOs occupy large chip areas due to the large size of the spiral inductors especially for the low GHz range (see figure 8). The inductor size scales down for higher oscillation frequencies but are still
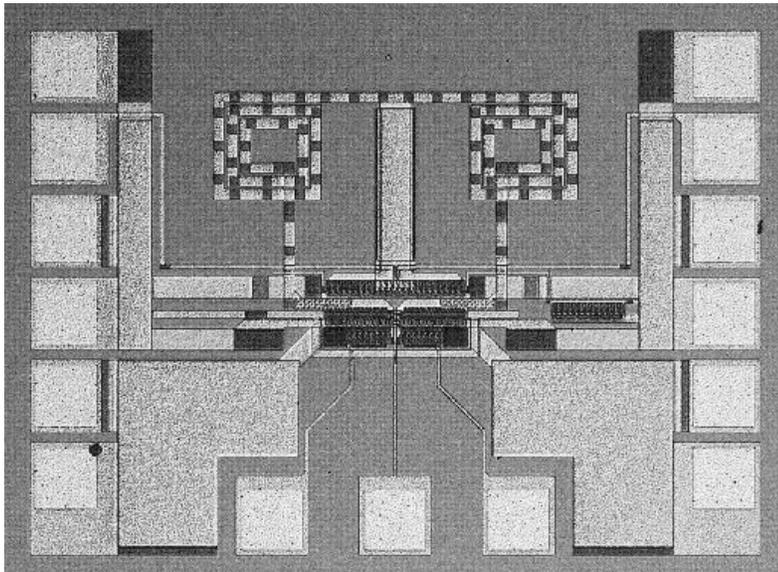
Figure 8: Microphotograph of a fully integrated 0.35um CMOS VCO operating at 5 GHz from [24].

substantial. On the system level, this extra cost in silicon area can be traded for simpler packaging, less external components, smaller board size, and ease of use.

With the down-scaling of the technology feature sizes more interconnection levels must be provided to enable higher digital circuit densities. Also, in deep sub-micron technologies the speed of digital circuits is interconnect-delay limited rather than transistor-delay limited which results in the introduction of low resistivity interconnects (e.g. Cu-based). These trends are favorable for the development of high quality on-chip integrated inductors [27].

- It is remarkable that the fully integrated oscillators with *bipolar active devices* ("LC/Bip" in figure 6) in a BiCMOS technology perform less good than the oscillators with MOS devices ("LC/CMOS" in figure 6). This is in contrast to the general belief that bipolar devices are preferable for RF circuits. A possible explanation lies in one extra complication a bipolar oscillator design has to deal with: possible conduction losses due to base-collector forward bias, whereas in a MOS device the gate terminal is always isolated. Therefore bipolar oscillators either include an extra buffer device for level shifting (see figure 9(a)) or use capacitive tapping (see figure 9(b)) to reduce the voltage swings across base-collector. The extra device introduces more noise sources in the oscillator core and capacitive tapping is unfavorable for the phase noise - power trade-off.
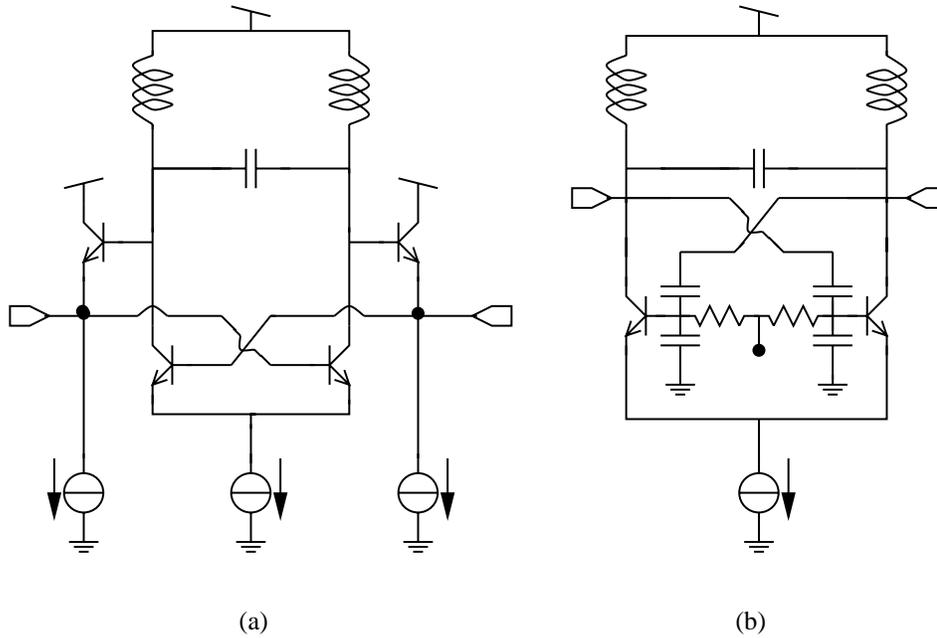
(a)   (b)

Figure 9: Bipolar implementations of a negative conductance. To avoid lossed due to base-collector forward bias either an emitter follower is used as level shifter (b), or capacitive tapping is used to reduce the signal swing at the base (c).

We have to note however that most of the listed bipolar VCO designs provide high output power and have good output buffering. In some topologies this buffering comes at very little extra power consumption. Most of the listed MOS VCOs do not include strong output buffering and are designed to drive on chip loads only.

Two oscillators using a *SiGe bipolar device* are listed ("LC/SiGe" in figure 6). Interestingly both perform better than the other bipolar VCOs even though they operate at higher frequencies. This could indicate that the BiCMOS VCOs also suffer from the typically fairly high base spreading resistance.

There is one important benefit of bipolar VCOs though that is not apparent from table 2: 1/f noise. Bipolar devices exhibit much lower 1/f noise than MOS devices so that the close-in noise sidebands for bipolar VCOs are lower than for MOS VCOs. The quadratic scaling with Δf assumes only white noise and does not account for the role of 1/f noise.

- Table 2 and figure 6 also include a group of *coupled oscillators* ("LC/Coup"). They consist of two coupled tuned oscillators where the coupling arrangement is typically such that the waveforms of the two oscillators are in quadrature (90 degrees out of phase). Accurate quadrature signals are essential for the realization of image reject mixers for highly integrated

transceivers [3, 4] and coupled oscillators can deliver very accurate quadrature signals. Coupled oscillators can also be used to build controllable oscillators without the need for varactors. However, their FM is significantly lower than that of other integrated oscillators even though in table 2 only the power consumption of one oscillator stage of the coupled oscillators is taken into account. This is due to the addition of extra devices to the oscillator core and thus extra noise sources.

5 Conclusions

With the advent of higher communication data rates and digital clock rates and the proliferation of wireless terminals the demand for integrated GHz oscillators is growing. Whereas for digital and data applications fully integrated ring oscillators are being widely used, the use of fully integrated tuned oscillators is only emerging in wireless products. Performance concerns as well as large area still inhibit the widespread acceptance of integrated tuned oscillators. The reduction of the number of RF interfaces in the package, the ease of use of fully integrated parts, compact board size and the implementation of automatic trimming techniques will however outweigh the extra die cost for large volume wireless terminals. The good performance of MOS oscillators and the introduction of better interconnect technologies in deep submicron technologies holds interesting prospects for highly integrated transceivers combining RF and analog front-ends with digital signal processing back-ends. The constant move to higher bit-rates will require a shift from non-tuned ring oscillators to fully integrated tuned oscillators for data and digital applications.

6 Acknowledgments

Type	f_0 [GHz]	$L\{\Delta f\}$ [dBc/Hz]	Δf [kHz]	Tune [%]	Vdd [V]	Idd [mA]	P [mW]	FM	Technology	#M	Sub	L	QL	QV
Vari-L VCO690-5800	module	5.800	-105.0	100	5.5	5.0	2.4	11.9	189.5						
Z-Comm v585me06	module	2.000	-100.0	10	66.7	10.0	5.0	50.0	189.0						
Wang ISSCC 99	LC/CMOS	9.800	-118.0	1000		2.2	5.5	12.0	187.0	CMOS035	4	LR	Inte L	5	
Huang CICC 98	LC/ext	0.926	-112.7	100		3.0	1.6	4.7	185.3	CMOS04			Discr L		
Murata MQH	module	1.686	-103.0	50	2.2	3.0	2.3	7.0	185.1						
Murata MQE	module	0.706	-115.0	100	0.6	3.2	1.6	5.0	185.0						
Kinget ESSCIRC 98	LC/ext	2.450	-124.0	1000	5.0	2.7	2.0	5.4	184.5	CMOS035	4	MCM	MCM L	70	
Dec ISSCC 99	LC/ext	1.900	-126.0	600	9.0	2.5	6.0	15.0	184.3	CMOS			Bondw	80	
Craninckx CICC 97	LC/CMOS	1.800	-113.0	200	20.0	3.0	3.0	9.0	182.5	CMOS04		HR	Inte L	8.6	
Craninckx ISSCC'94	LC/ext	1.800	-115.0	200	5.0			24.0	180.3	CMOS07	2	LR	Bondw	80	
Mini-C JTOS-1910	module	1.910	-132.0	1000	16.1	12.0	6.6	79.2	178.6						
CTI VMS	module	2.500	-90.0	25	23.2	5.0	2.8	14.2	178.5						
Plouchart ESSCIRC 98	LC/SiGe	6.000	-116.0	1000	14.9	3.1	7.1	22.0	178.1	SiGe BiCMOS	3/T	HR	Inte L	11	30
Murata MQG	module	2.138	-90.0	25	3.8	3.0	4.0	12.0	177.8						
Craninckx VLSI 96	LC/CMOS	1.800	-116.0	600	12.0	1.5	4.0	6.0	177.8	CMOS07	2	LR	Inte L	5.7	
Craninckx CICC 97	LC/CMOS	0.900	-108.0	100	20.0	3.0	3.7	11.0	176.7	CMOS04	2	HR	Inte L	5.6	
Plouchart ESSCIRC 98	LC/SiGe	17.380	-104.8	1000	3.6	3.1	7.1	22.0	176.2	SiGe BiCMOS	3/T	HR	Inte L	12	
Dauphinee ISSCC 97	LC/Bip	1.500	-105.0	100	10.0	3.6	7.8	28.0	174.1	BiCMOS08/11GHz			Inte L	5	
Kinget ISSCC 98	LC/CMOS	5.200	-90.0	100	4.0	2.7	4.0	10.8	174.0	CMOS035	4	LR	Inte L	3	
Jansen ISSCC 97	LC/Bip	2.200	-99.0	100	12.0	2.7	8.0	21.6	172.5	Bipolar 15GHz			Inte L	10	30
Waegemans ISSCC 98	LC/Bip	1.800	-112.0	2000	0.7			1.0	171.1	Bipolar		glass	Inte L		
Soyeur ISSCC 96	LC/Bip	4.100	-106.0	1000	9.0	3.0	8.0	24.0	164.5	BiCMOS	5/T		Inte L	7	
Rofourgaran ISSCC 96	LC/etch	0.820	-100.0	100	14.0			25.0	164.3	CMOS1	2	etch	Inte L	5	
Basedau Esscirc 94	LC/etch	1.000	-95.0	100	0.0			16.0	163.0	CMOS10		etch	Inte L		
Soyeur VLSI 94	LC/Bip	2.400	-92.0	100	0.0	0.0	0.0	50.0	162.6	BiCMOS	4/T		Inte L		
Razavi ISSCC 97	LC/Coup	1.800	-100.0	500	7.0	3.3	2.3	7.6	162.3	CMOS06	3		Inte L		
Liu ISSCC 99	LC/Coup	6.290	-98.4	1000	16.9	1.5	12.0	18.0	161.8	CMOS035	4	LR	Inte L		
Kwasniewski CICC 95	Ring	0.740	-89.0	100	6.0			6.5	158.3	CMOS120					
Nguyen JSSC 90	LC/Coup	1.800	-88.0	100	10.0			70.0	154.7	Bipolar 10GHz			Inte L		

Table 2: Performance of VCOs in different implementation styles

	Type	f_0 [GHz]	$L\{\Delta f\}$ [dBc/Hz]	Δf [kHz]	Tune [%]	Vdd [V]	Idd [mA]	P [mW]	FM	Technology	#M	Sub	L	QL QV
Hajimiri CICC 98	Ring	2.810	-95.2	1000				10.0	154.2	CMOS025				
Hajimiri CICC 98	Ring	5.430	-98.5	1000	25.0			80.0	154.2	CMOS025				
Lam ISSCC 99	LC/Coup	2.600	-110.0	5000	12.3	2.5	5.2	13.0	153.2	CMOS035	4			
Sneep JSSC90	Relax	0.100	-118.0	1000	100.0			30.0	143.2	Bipolar 3GHz			Inte L	
Banu JSSC 88	Relax	0.560	-90.0	500	100.0			50.0	134.0	CMOS075				

Table 2: Performance of VCOs in different implementation styles

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